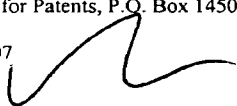


U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/85	
Application Number 10/791,501	Filing Date March 1, 2004	Examiner James K. Trujillo	Art Unit 2116
Invention Title RUNTIME CONFIGURABLE ARITHMETIC AND LOGIC CELL		Inventor Martin VORBACH et al.	

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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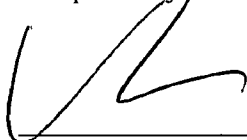
Date: August 28, 2007

Signature: 
Michelle M. Carniaux (Reg. No. 36,098)

SIR:

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 35 U.S.C. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby brings the following references to the attention of the Examiner. These references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.
2. The filing of this Information Disclosure Statement and the enclosed PTO 1449 shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. §1.56(b).
3. A copy of each patent, publication or other information listed on the modified PTO 1449 is enclosed, except for United States patent references or where indicated on the list of references (Form 1449).
4. It is believed that no fees are due in connection with this Information Disclosure Statement. However, should any fees be due, the Commissioner is authorized to charge Deposit Account No. 11-0600 for such fees. A duplicate of this communication is enclosed for charging purposes.

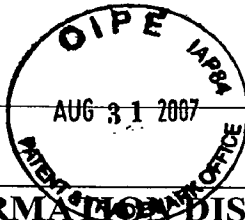
Respectfully submitted,



Dated: August 28, 2007

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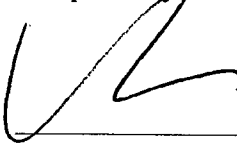
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INFORMATION DISCLOSURE STATEMENT BY APPLICANTS

PTO 449

AUG 31 2007



Attorney Docket No.
2885/85

Serial No.
10/791,501

Applicant(s)
Vorbach et al.

Filing Date
March 1, 2004

Group Art Unit
2116

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INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449

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	0 463 721	January 2, 1992	EPO				
	0 539 595	May 5, 1993	EPO				
	0 696 001	December 5, 2001	EPO				
	9-27745	January 28, 1997	Japan			Abstract	
	11-307725	November 5, 1999	Japan			Abstract & Partial Translation	
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	Chen et al., "A reconfigurable multiprocessor IC for rapid prototyping of algorithmic-specific high-speed DSP data paths," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 27, No. 12, December 1992, pp.1895-1904.
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	John, L., et al., "A Dynamically Reconfigurable Interconnect for Array Processors," Vol. 6, No. 1, March 1998, IEEE, pages 150-157.

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EXAMINER /Nitin Patel/

DATE CONSIDERED 05/29/2008

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.